UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,711	02/02/2004	Paul J. Steffan	H0897	2278

22898 7590 11/13/2006

THE LAW OFFICES OF MIKIO ISHIMARU
333 W. EL CAMINO REAL
SUITE 330
SUNNYVALE, CA 94087

EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/770,711	STEFFAN, PAUL J.	
	Examiner	Art Unit	
	Magid Y. Dimyan	2825	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is with regards to the Amendment after Final Rejection, and Remarks, filed 10/02/2006. Applicant has amended claims 1 – 20. Claims 1 – 20 remain pending in this Application.

Response to Remarks

2. Applicant's remarks/arguments with respect to the rejections of claims 1 - 20 under 35 U.S.C 102 (b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of U.S. Patent No. 6,507,933 B1 to Kirsch et al.

3. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 20 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,507,933 B1 to Kirsch et al. (hereinafter, "Kirsch").

6. Referring to claims 1 and 11, Kirsch teaches a method (claim 1) and a system (claim 11 – Abstract; col. 2, ll. 59 - 67) for facilitating semiconductor wafer lot disposition (see col. 2, ll. 3 - 22) comprising: a) providing detailed descriptive information of the

semiconductor wafer layout (see col. 1, ll. 11 – 21; col. 11, ll. 52 - 58, which cite ASIC and semiconductor wafers and dies of integrated circuits in manufacture; IC's can only be manufactured by providing detailed descriptive information of a layout); (b) locating and defining current defects in partially completed dies of a semiconductor wafer in a wafer production lot to generate data concerning at least one defect in the semiconductor wafer at an intermediate processing stage (see col. 2, ll. 8 - 12); (c) generating at least one layer model from the information and data to disclose the effects of the defect upon at least one later layer of the semiconductor layer (see col. 2, ll. 3 – 22; col. 2, ll. 35 -41); and (d) utilizing the layer model to determine the subsequent disposition of the wafer production lot (see again col. 2, ll. 3 – 50; col.). Kirsch therefore clearly discloses, or at the very least suggests, the claimed limitations.

7. Pursuant to claims 2 and 3 see col. 2, ll. 31 – 40; col. 2, ll. 59 – 67; col. 5, ll. 1 - 30, which suggest the limitations pertaining to generating and utilizing a layer model (i.e., defect signature) to determine subsequent disposition of the wafer production lot (claim 3), and suggesting the locations of components above a defect in a wafer (claim 2).

8. As for claim 4, see items (4) and (5) above, as well as col. 4, ll. 44 - 67, which cite the likely cause and clustering of possible defects in a production wafer lot, as claimed.

9. Referring to claim 5, see again col. 11, ll. 41 – 58, which teach computer program for laying out an ASIC or standard cell design which require a netlist in order to perform the layout.

10. With regards to claims 6 and 16, Kirsch teaches a method (claim 6) and a system (claim 16 – see also item (4) above) for facilitating semiconductor wafer lot disposition (see item (4) above) comprising: a) providing detailed descriptive information of the semiconductor wafer layout (see item (7) above); (b) locating and defining current defects in partially completed dies of semiconductor wafers in a wafer production lot to generate and extract data concerning defects in the semiconductor wafers at an intermediate processing stage (see item (4) above); (c) generating at least one layer model from the information and data to disclose the future effects of the current defects upon later layers at subsequent stages of the process(see item (4) above); and (d) utilizing the layer model to determine the subsequent disposition of the wafer production lot (see again item (4) above). Kirsch therefore discloses the claimed limitations.

11. Claims 7, 12 and 17 contain the same limitations as claim 2, and therefore the same rejections also apply.

12. Claims 8, 13 and 18 contain the same limitations as claim 3, and therefore the same rejections also apply.

13. Claims 9, 14 and 19 contain the same limitations as claim 4, and therefore the same rejections also apply.

14. Claims 10, 15 and 20 contain the same limitations as claim 5, and therefore the same rejections also apply.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Magid Y Dimyan
Examiner
Art Unit 2825

myd
08 November 2006

JACK CHIANG
SUPERVISORY PATENT EXAMINER